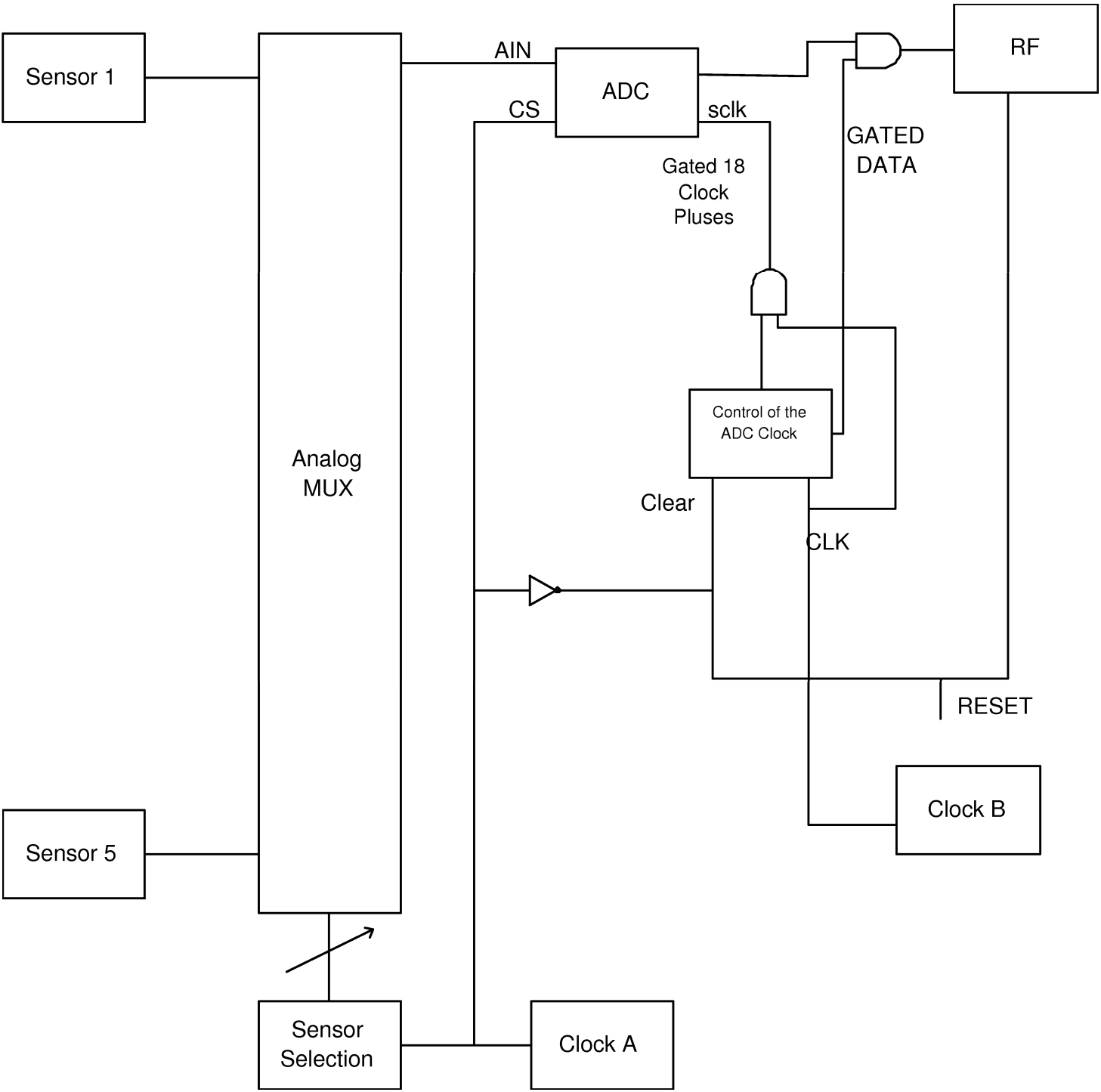
Sensor 1
Analog MUX
AIN
ADC
CS
sclk
RF
GATED DATA
Gated 18 Clock Pluses
Control of the ADC Clock
Clear
CLK
RESET
Clock B
Sensor 5
Sensor Selection
Clock A