

CpE358/CS381

**Switching Theory and
Logical Design**

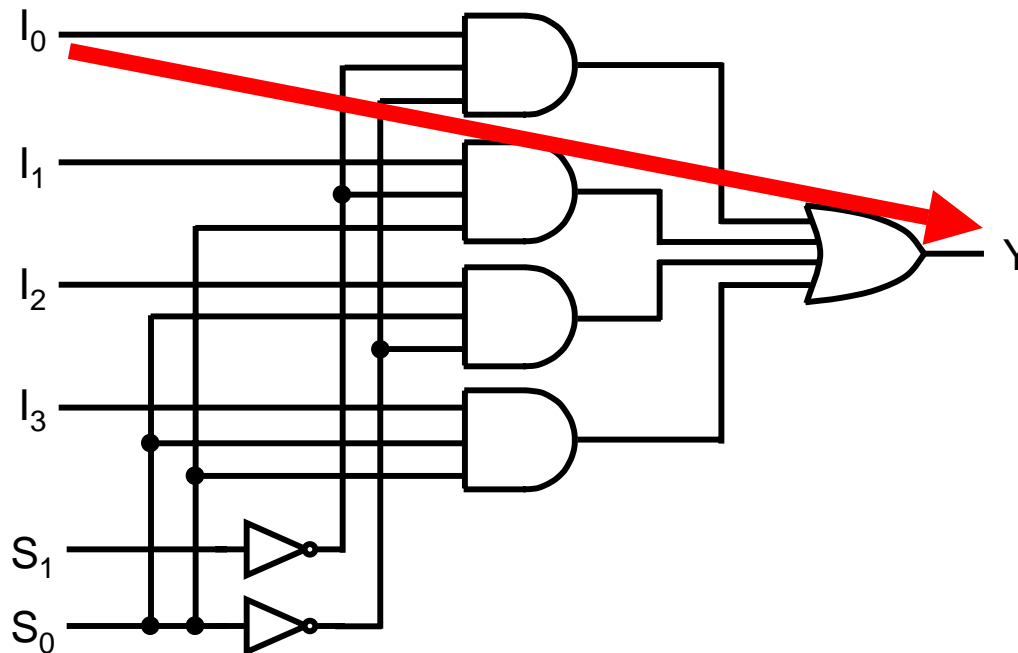
Class 6

Today

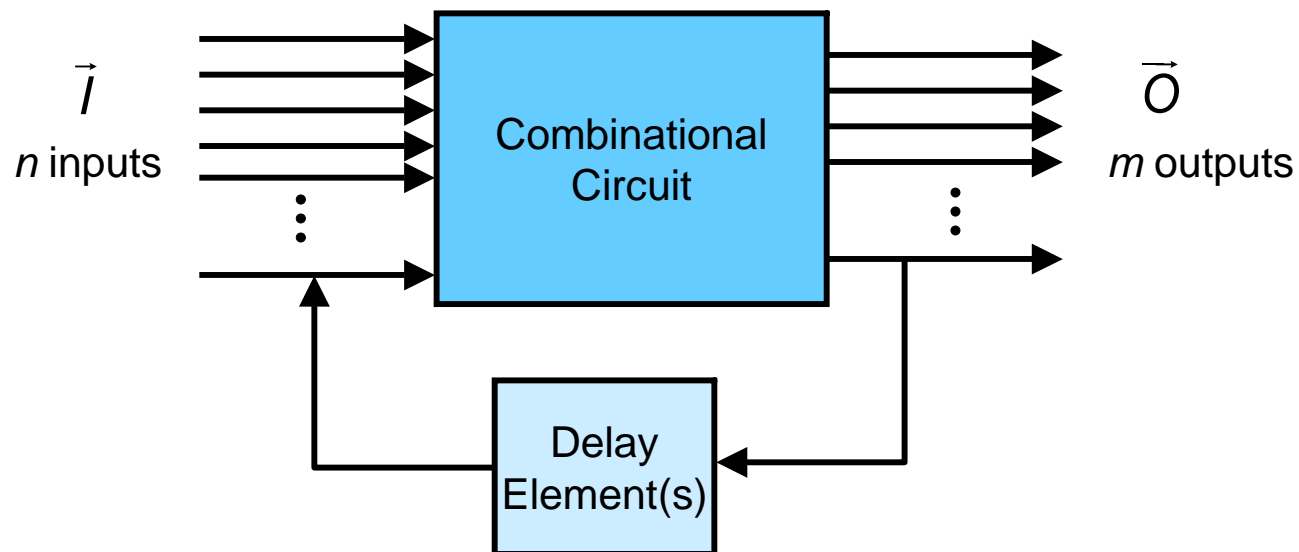
- Fundamental concepts of digital systems (Mano Chapter 1)
- Binary codes, number systems, and arithmetic (Ch 1)
- Boolean algebra (Ch 2)
- Simplification of switching equations (Ch 3)
- Digital device characteristics (e.g., TTL, CMOS)/design considerations (Ch 10)
- Combinatoric logical design including LSI implementation (Chapter 4)
- **Flip-flops and state memory elements (Ch 5)**
- **Sequential logic analysis and design (Ch 5)**
- Hazards, Races, and time related issues in digital design (Ch 9)
- Synchronous vs. asynchronous design (Ch 9)
- Counters, shift register circuits (Ch 6)
- Memory and Programmable logic (Ch 7)
- Minimization of sequential systems
- Introduction to Finite Automata

Characteristics of Combinatorial Circuits

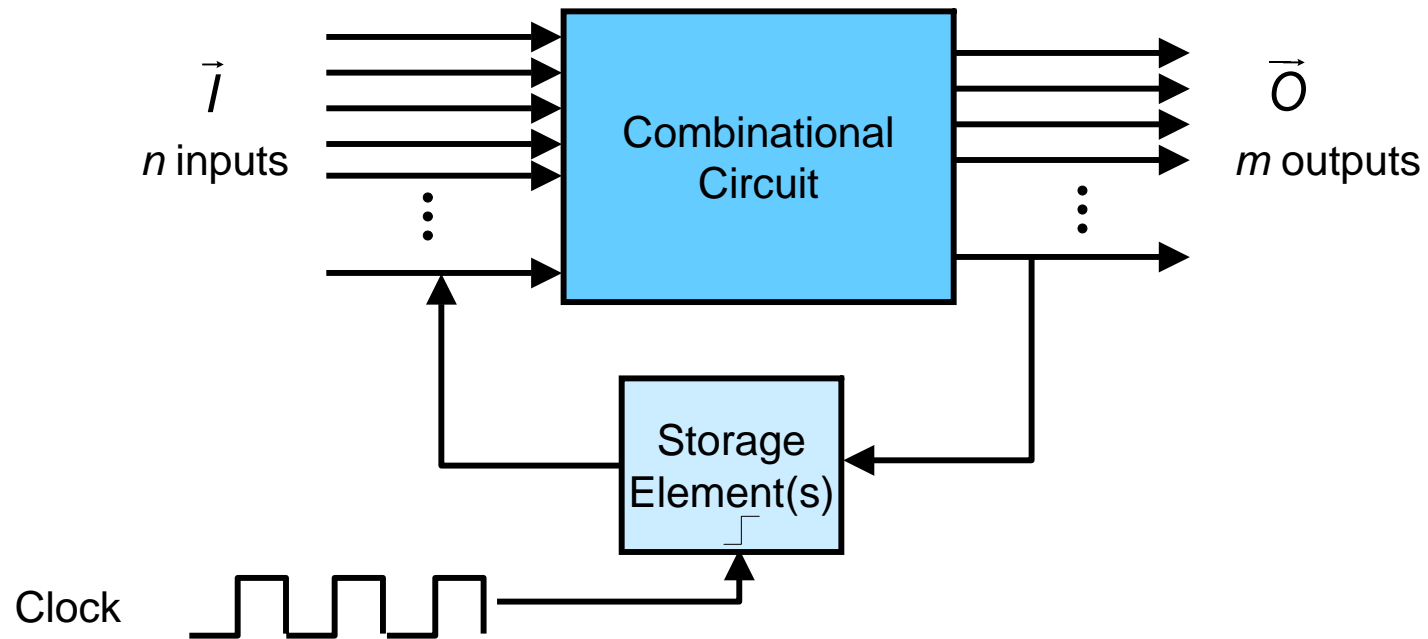
- Linear signal flow – input to output
- No feedback paths
- No storage elements



Asynchronous Sequential Circuit

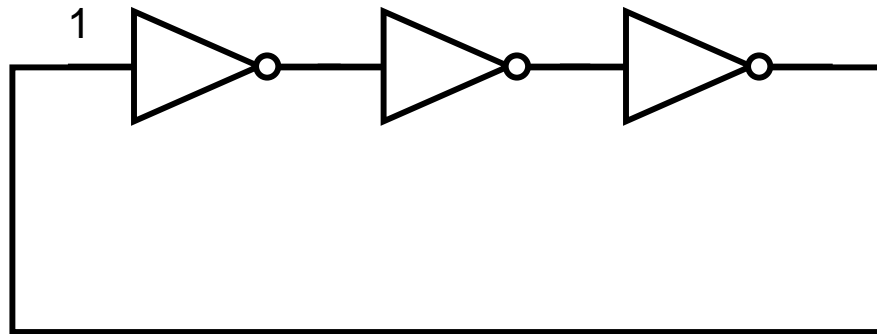


Synchronous Sequential Circuit



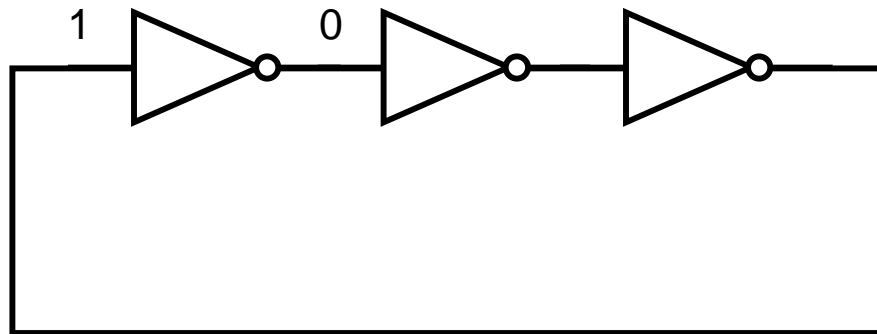
Feedback Paths in Logic Circuits

- Condition of signal leads is indeterminate



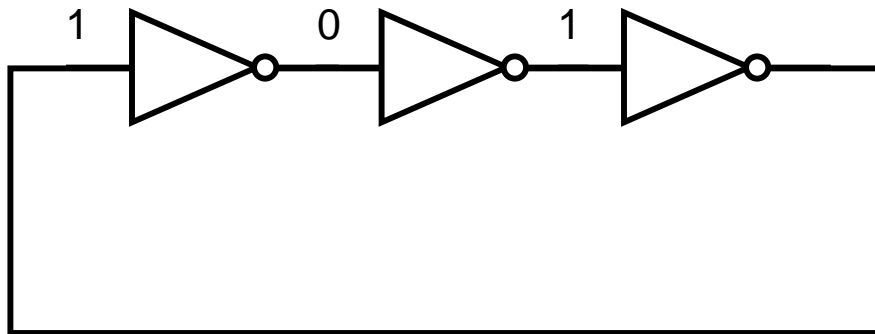
Feedback Paths in Logic Circuits

- Condition of signal leads is indeterminate



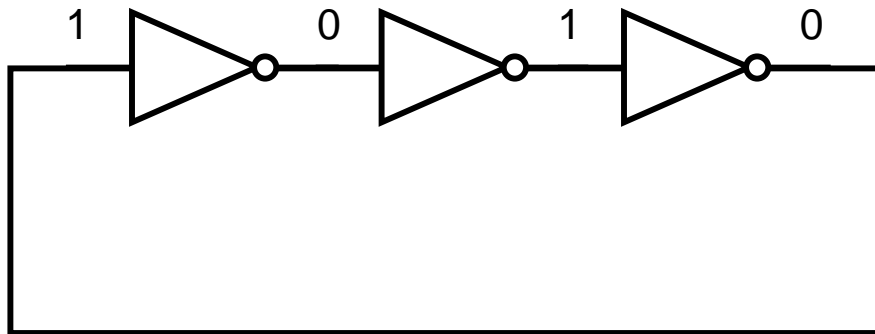
Feedback Paths in Logic Circuits

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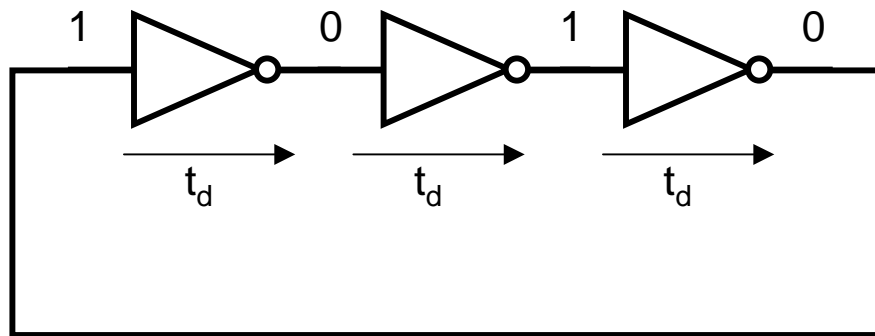
Feedback Paths in Logic Circuits

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Feedback Paths in Logic Circuits

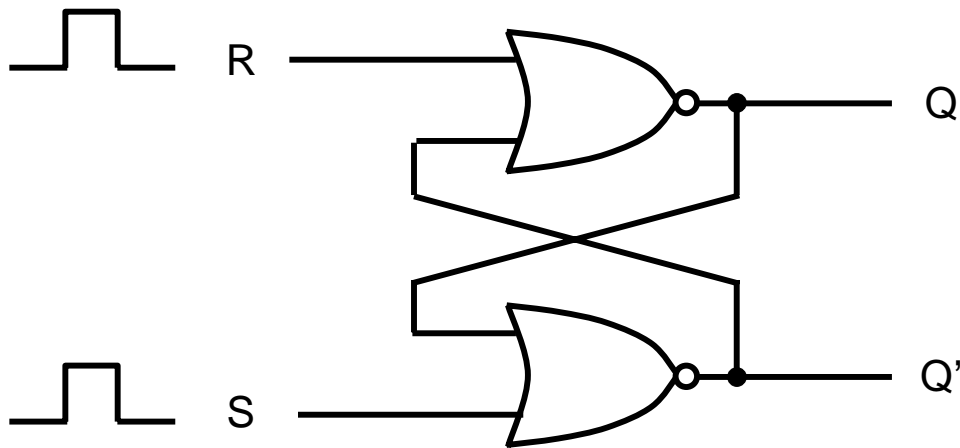
- Condition of signal leads is indeterminate



- With some technologies (e.g., CMOS) this can actually be used to build an oscillator ($f \sim 1/(3t_d)$)

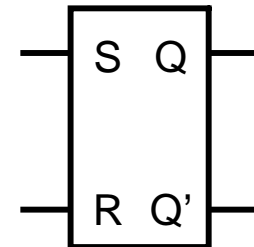
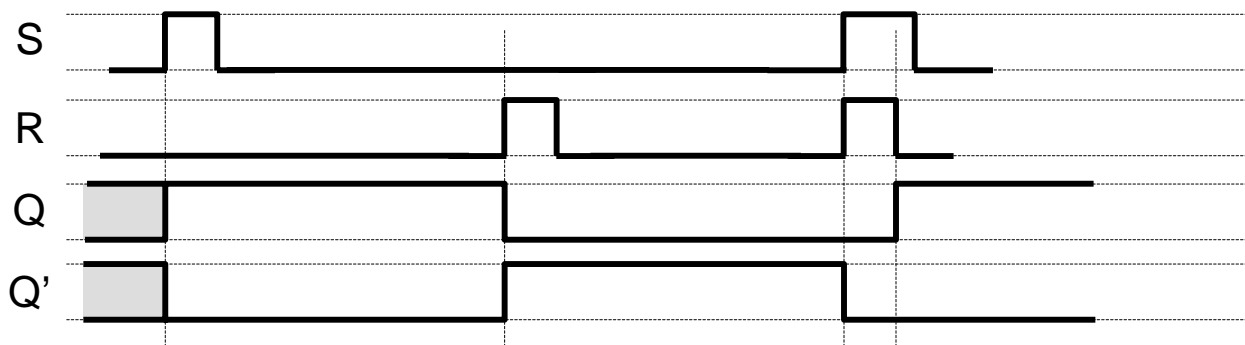
Basic Storage Element - Latches

• NOR gate "S-R" Latch



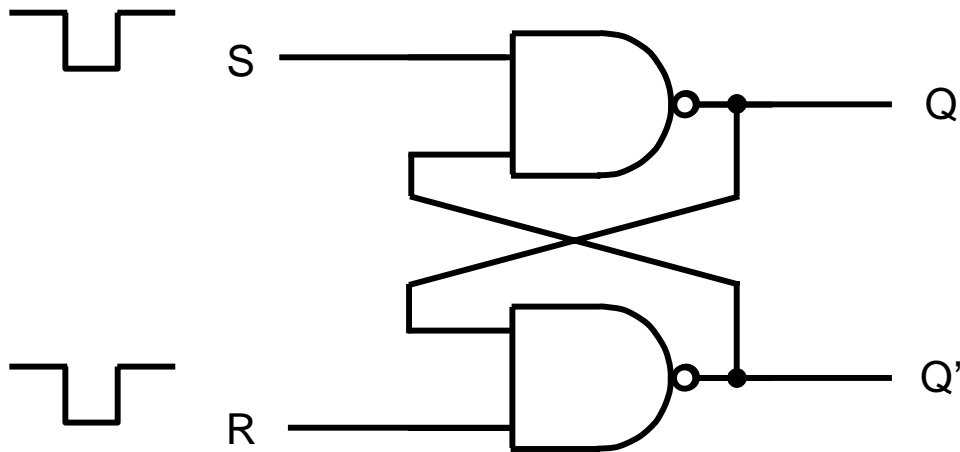
S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

Values Held



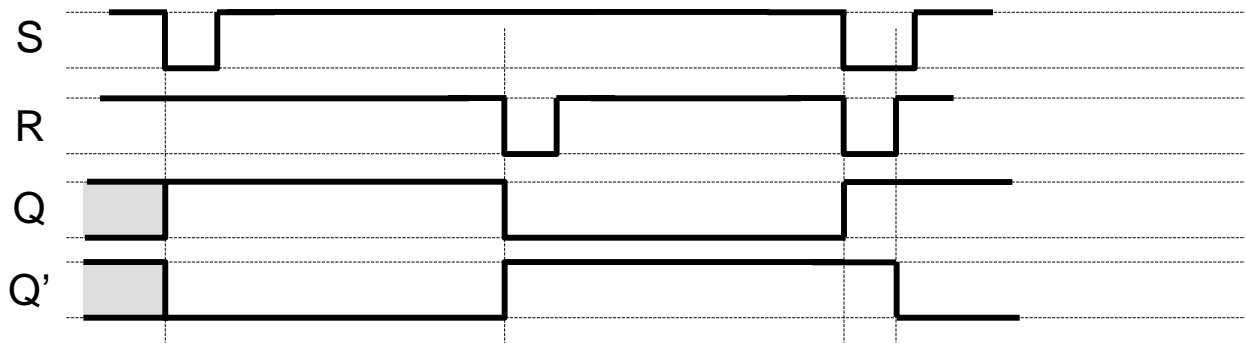
Basic Storage Element - Latches

- NAND gate "S-R" Latch



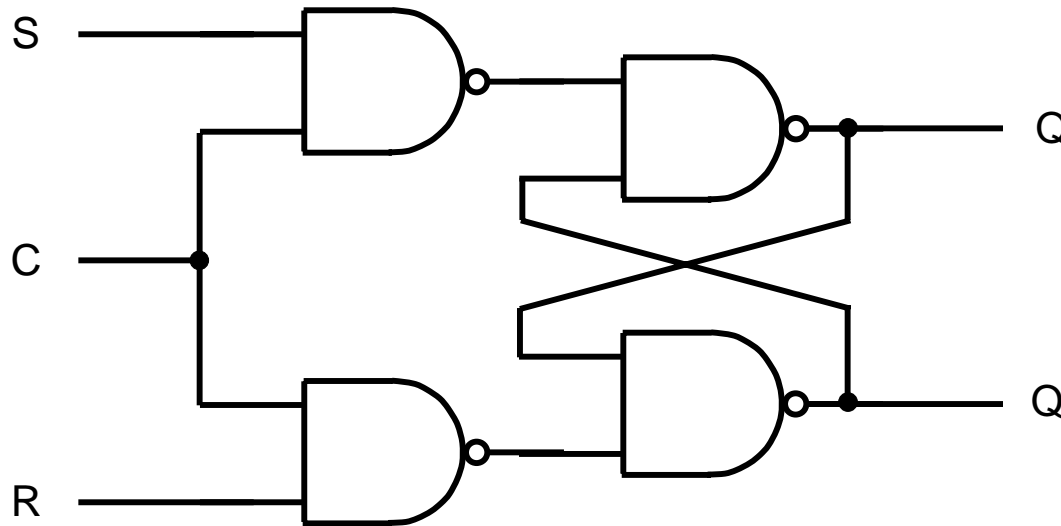
S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
1	1	1	1

Values Held

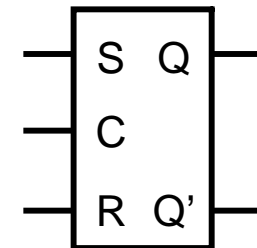
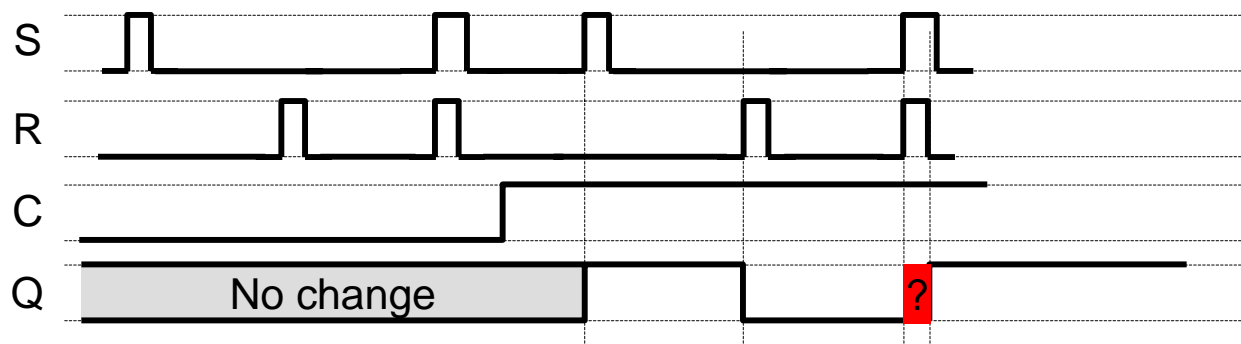


Basic Storage Element - Latches

- NAND gate “S-R” Latch with control input

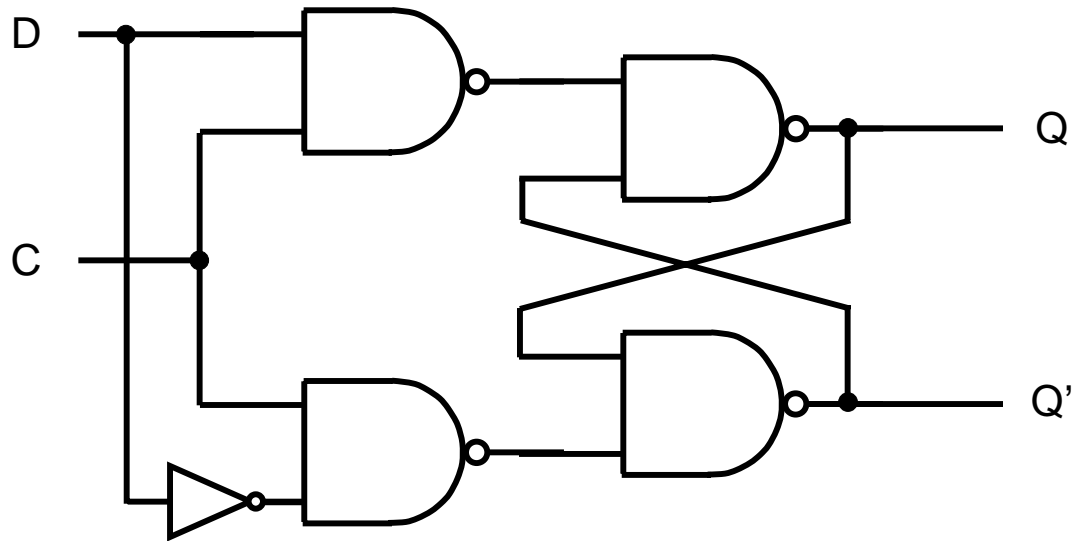


C	S	R	Q_{i+1}
0	X	X	Q_i
1	0	0	Q_i
1	0	1	0
1	1	0	1
1	1	1	?

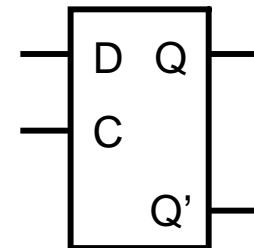
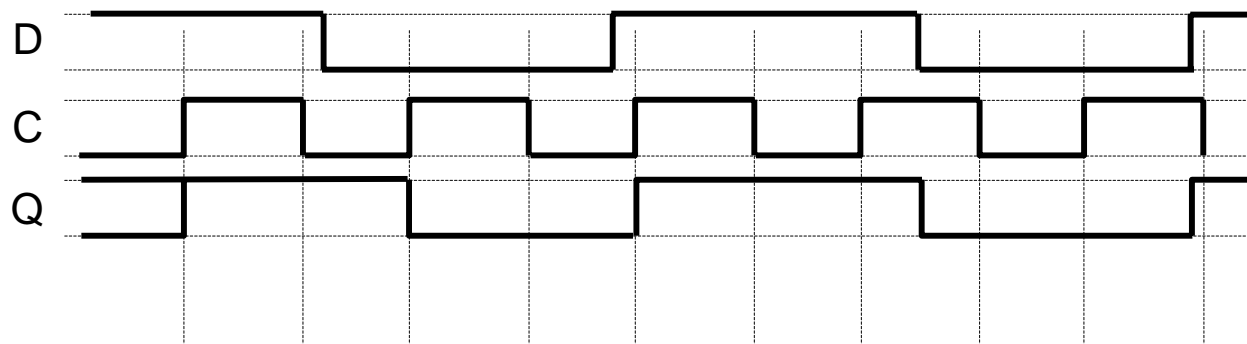


Basic Storage Element - Latches

- D Latch with control input

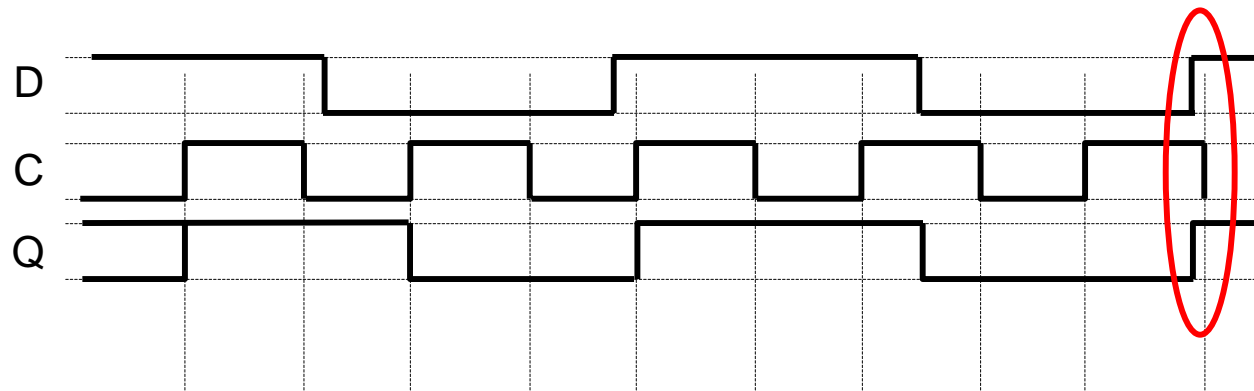


C	D	Q_{i+1}
0	X	Q_i
1	0	0
1	1	1

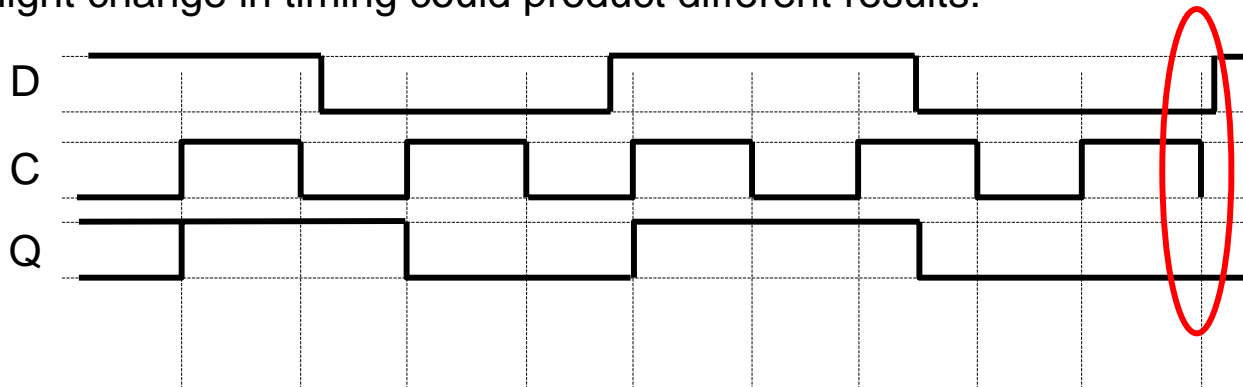


Limitations of Level Sensitive Latches

- What is timing of D vs. C?

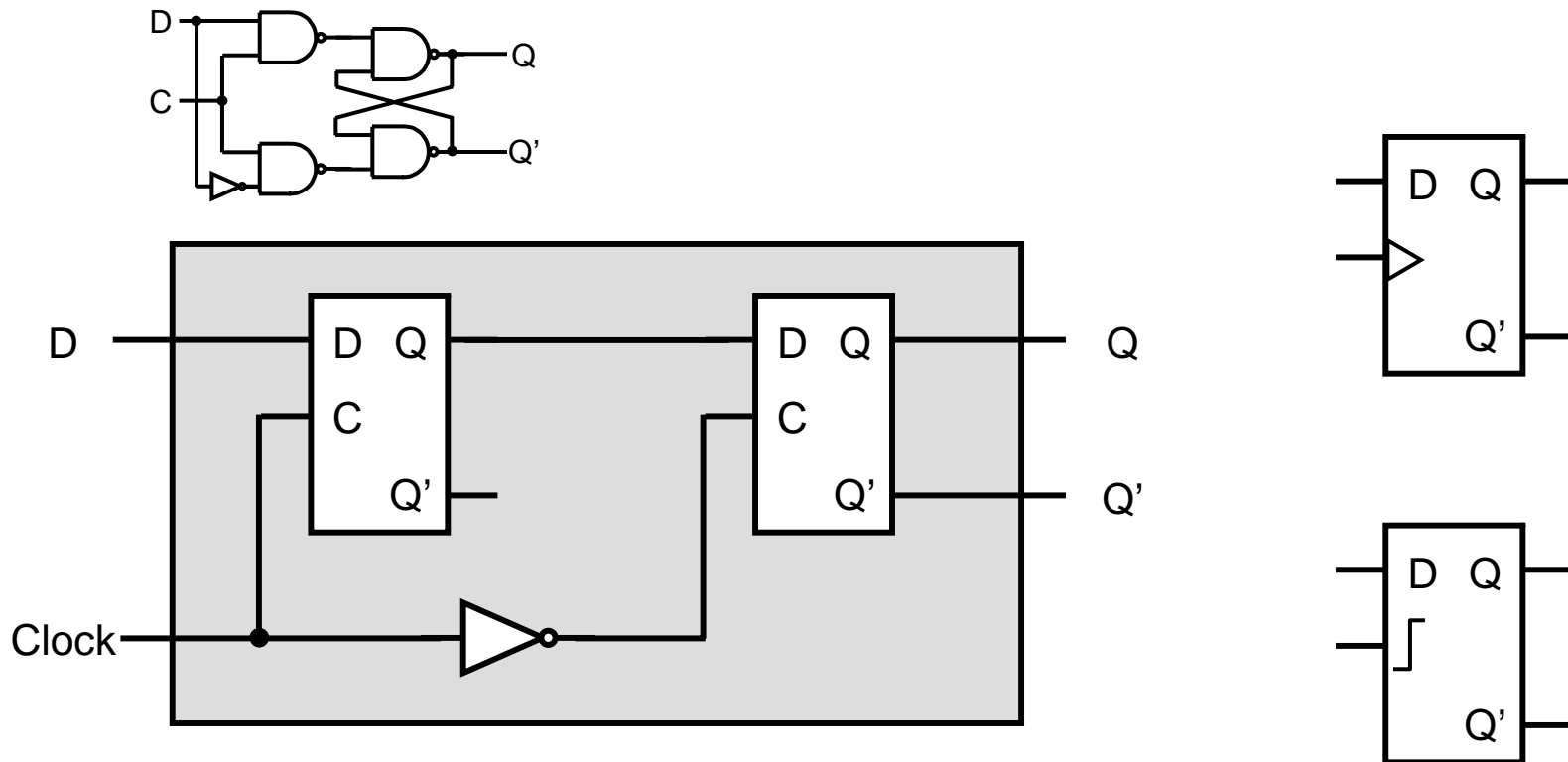


- A slight change in timing could produce different results:

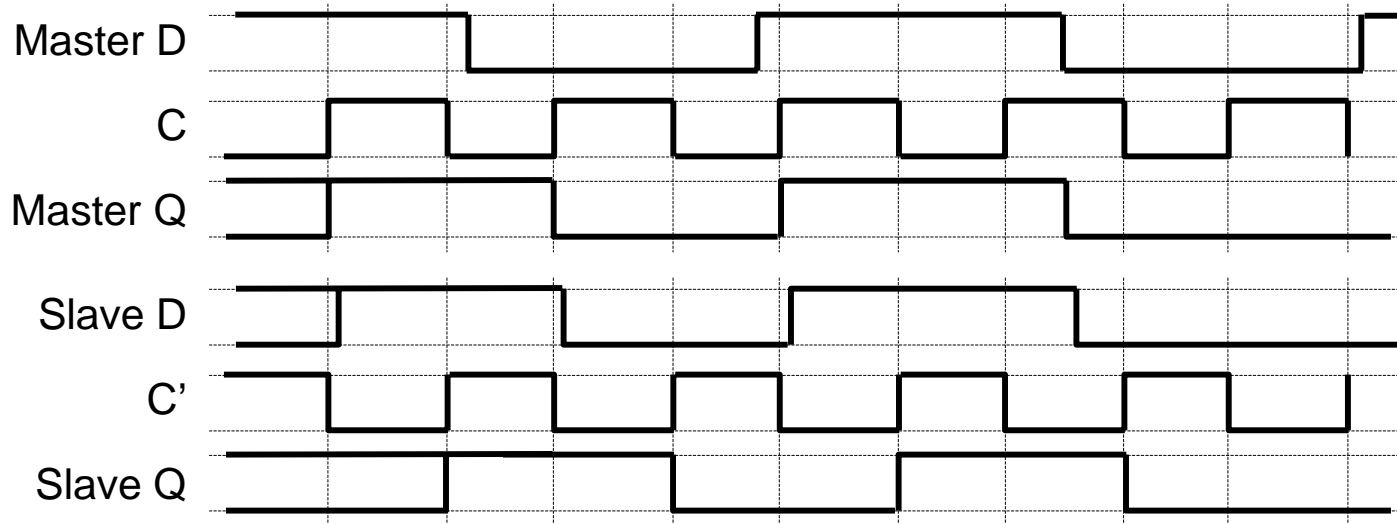
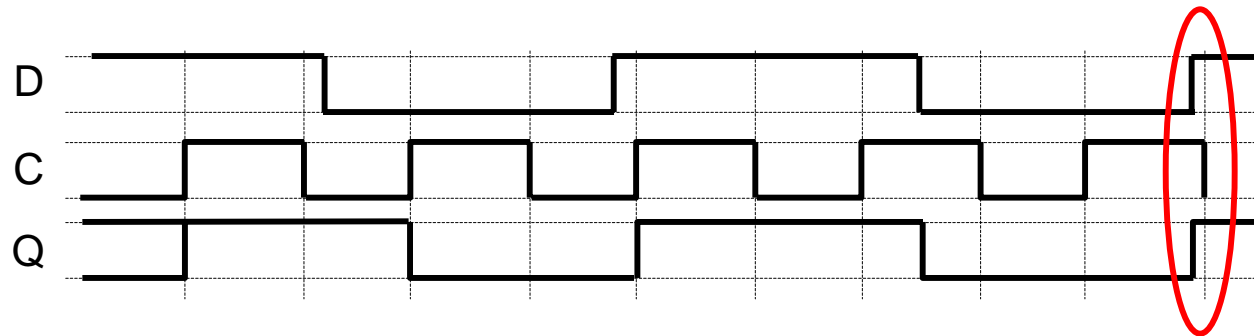


Master-Slave D Flip-Flop

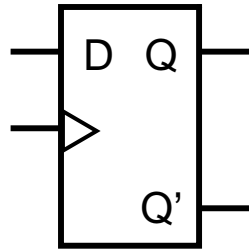
$$Q(t+1) = D$$



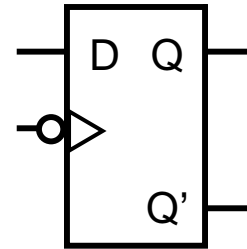
Master-Slave Timing



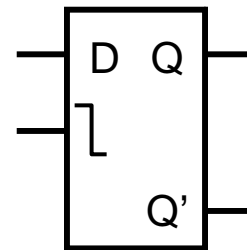
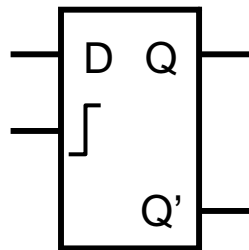
Variations of D Flop-flops



Positive Edge Triggered

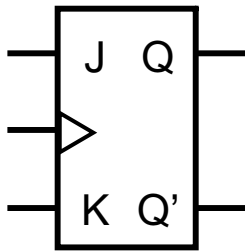


Negative Edge Triggered



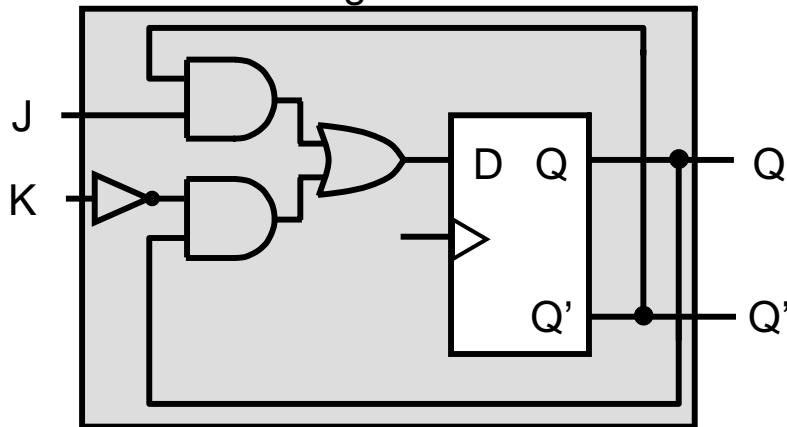
J-K Flip Flop

$$Q(t+1) = JQ' + K'Q$$

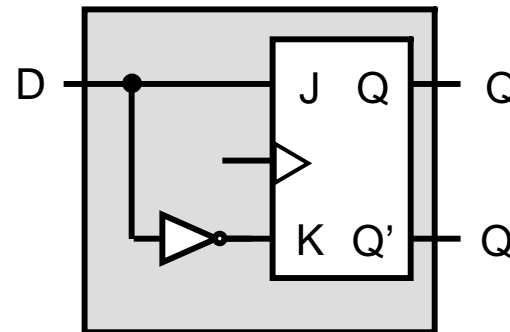


J	K	Q_{i+1}	Meaning
0	0	Q_i	No change
1	0	1	Clockin 1
0	1	0	Clockin 0
1	1	Q_i'	Toggle

Constructing a J-K from a D

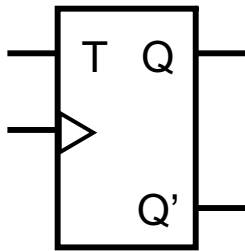


Constructing a D from a J-K



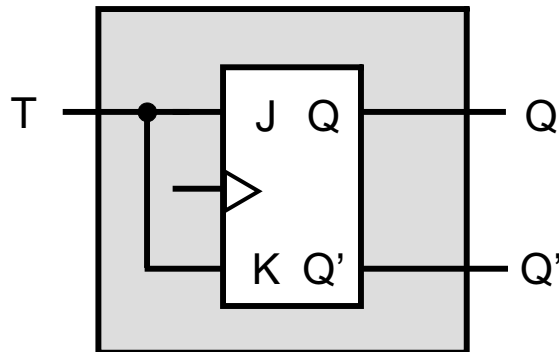
Toggle Flip Flop

$$Q(t+1) = T \oplus Q$$

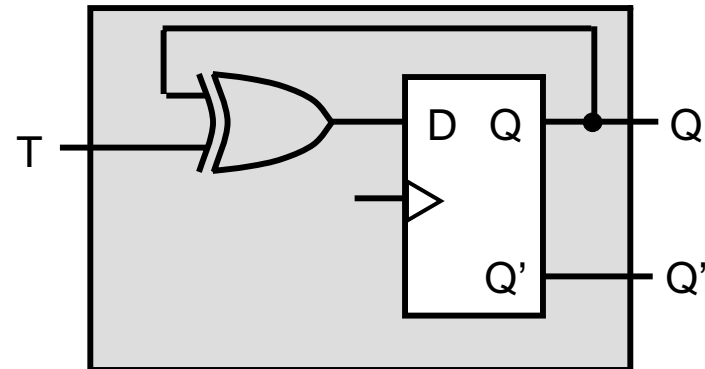


T	Q_{i+1}	Meaning
0	Q_i	No change
1	Q_i'	Toggle

Constructing a T from a JK

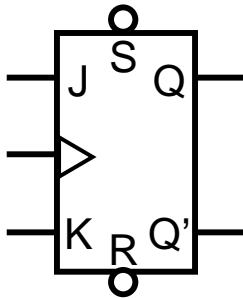


Constructing a T from a D



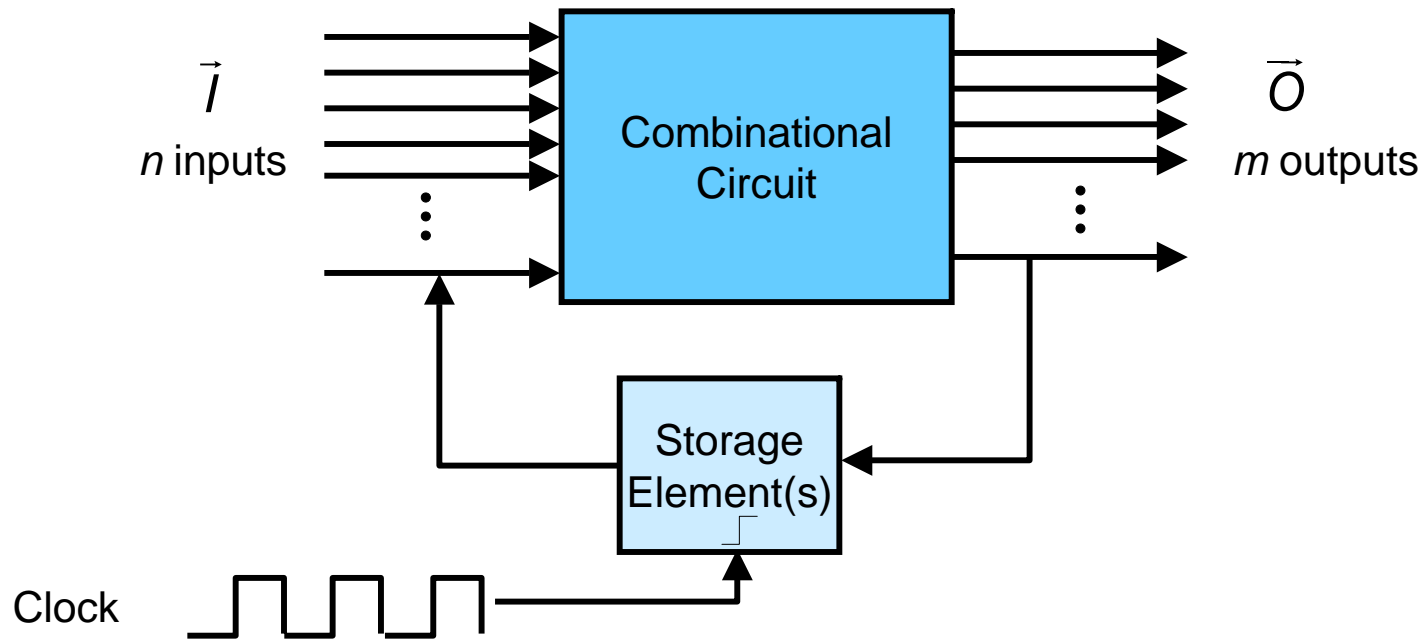
Immediate Inputs to Flip-Flops

- Sometimes referred to as Preset and Clear, the immediate inputs can be used to preset a known state at startup



J	K	S	R	Q_{i+1}	Meaning
0	0	1	1	Q_i	No change
1	0	1	1	1	Clockin 1
0	1	1	1	0	Clockin 0
1	1	1	1	Q_i'	Toggle
X	X	0	1	1	Set
X	X	1	0	0	Reset
X	X	0	0	?	Undefined

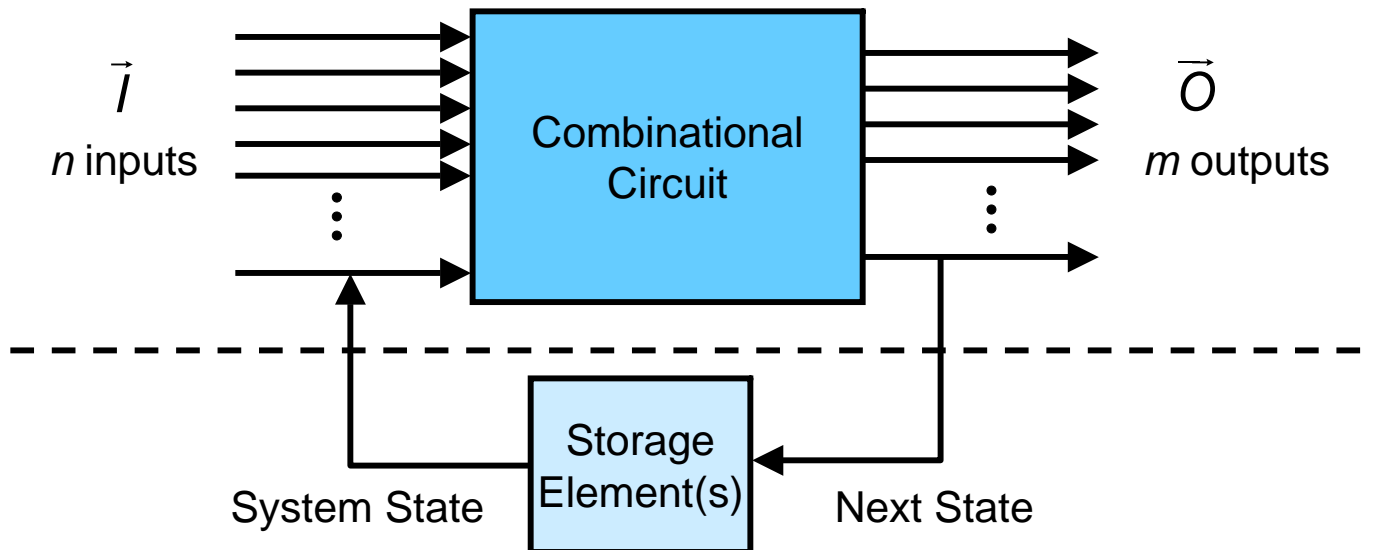
Generic Sequential Clocked Sequential Circuit



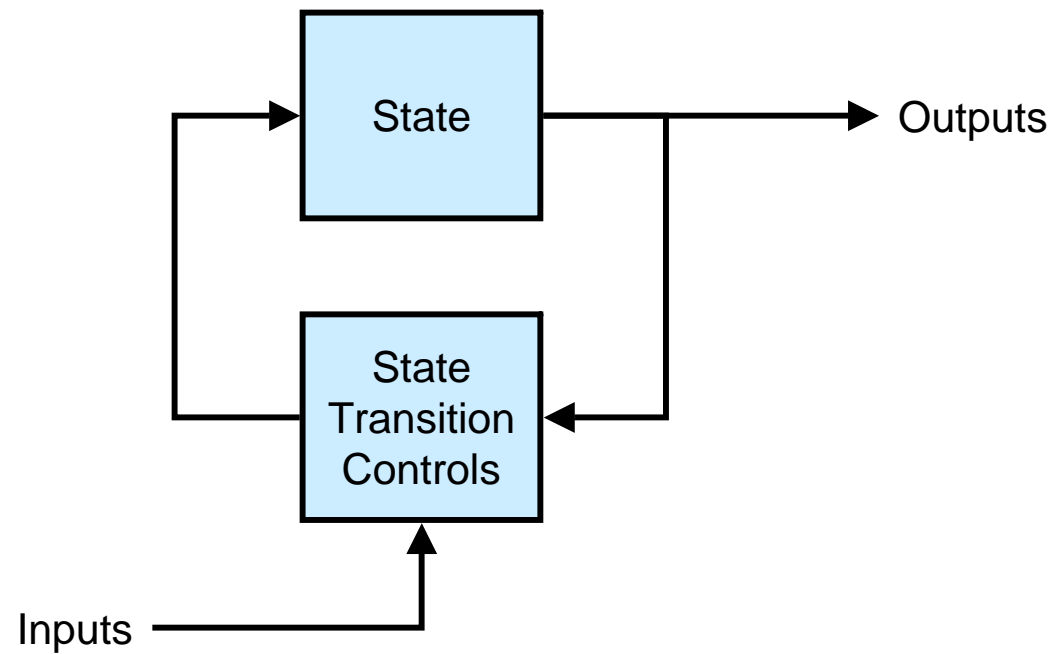
Generic Sequential Clocked Sequential Circuit

Storage elements contain system state

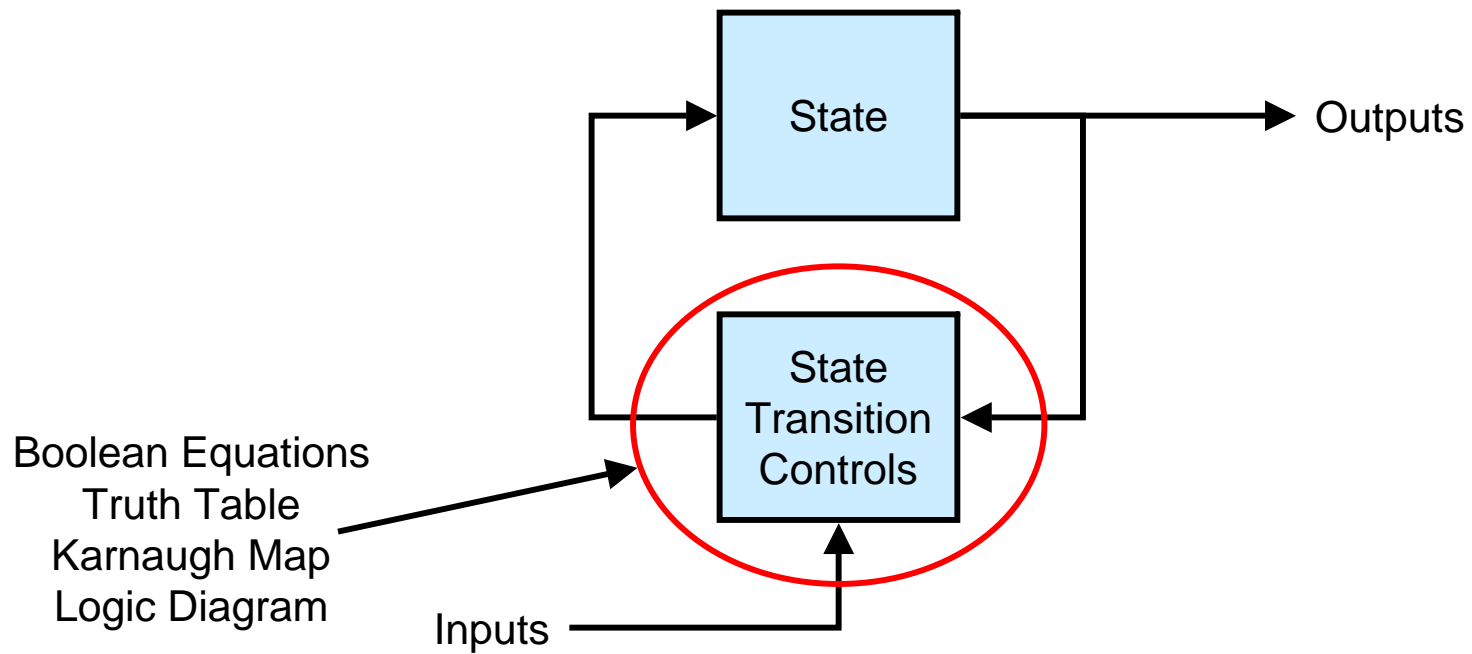
Combinational circuit determines next state



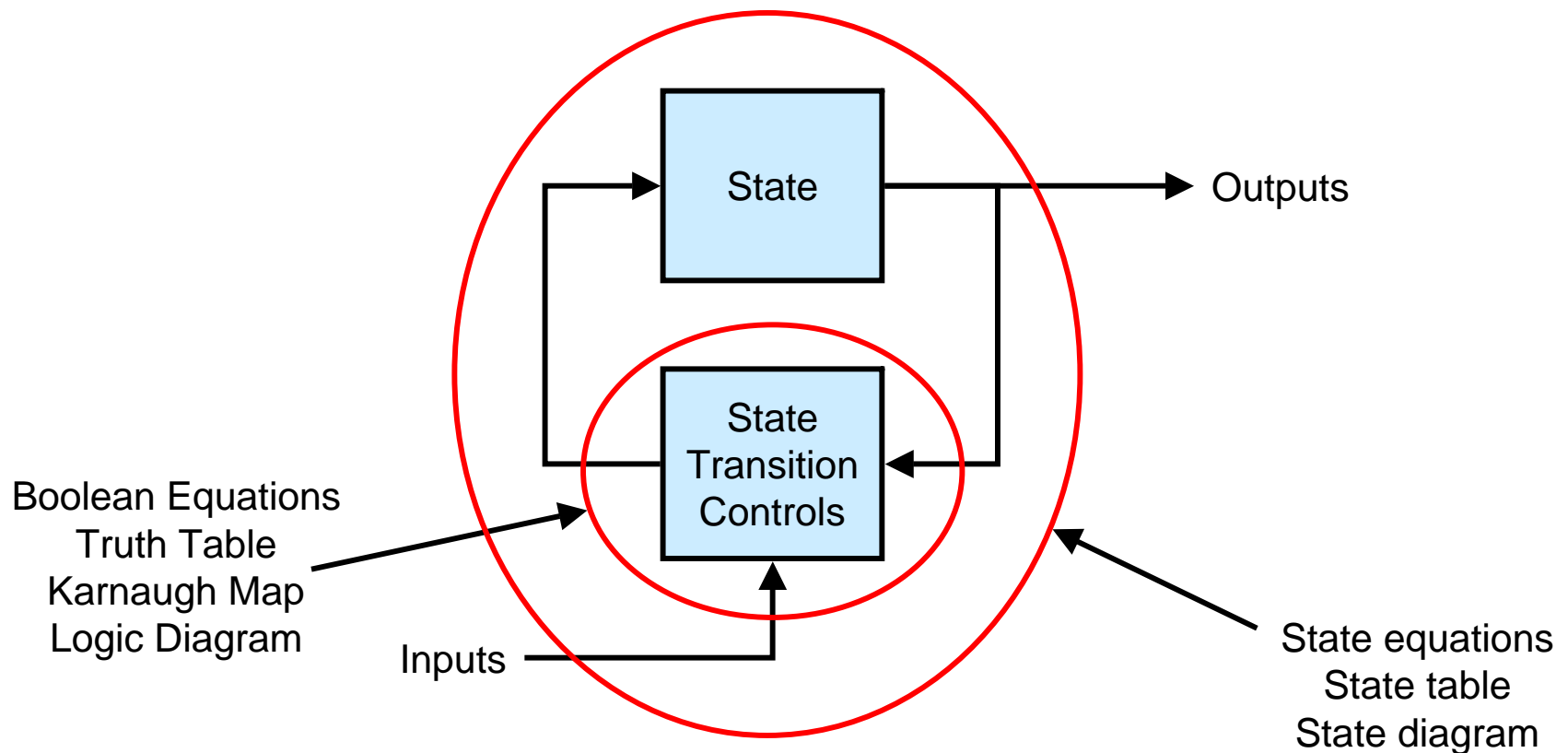
Abstraction of Sequential Circuit



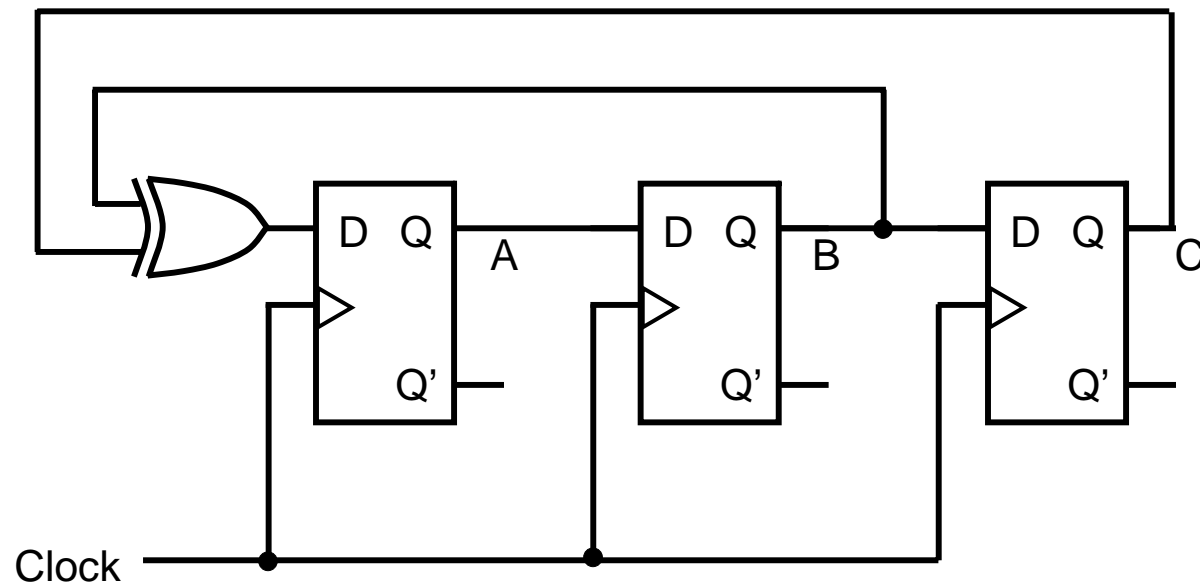
Abstraction of Sequential Circuit



Abstraction of Sequential Circuit

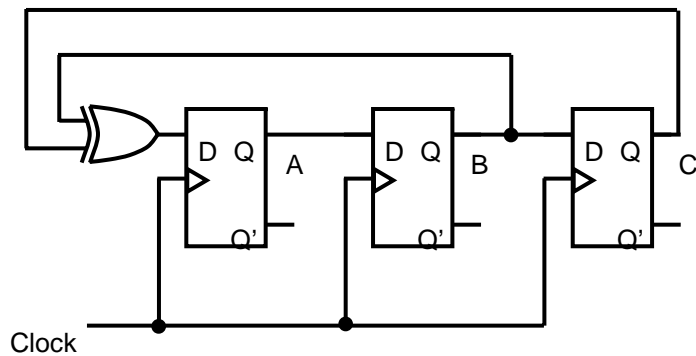


Typical Sequential Circuit With No Inputs



Typical Sequential Circuit With No Inputs

- Description by State Equations



$$A(t+1) = B(t) \oplus C(t)$$

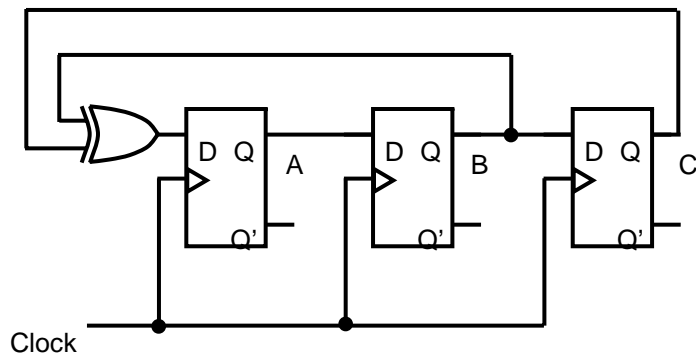
$$B(t+1) = A(t)$$

$$C(t+1) = B(t)$$

$$\begin{aligned} A(t+1) &= B(t+1) = A(t) \\ C(t+1) &= B(t) \end{aligned}$$

Typical Sequential Circuit With No Inputs

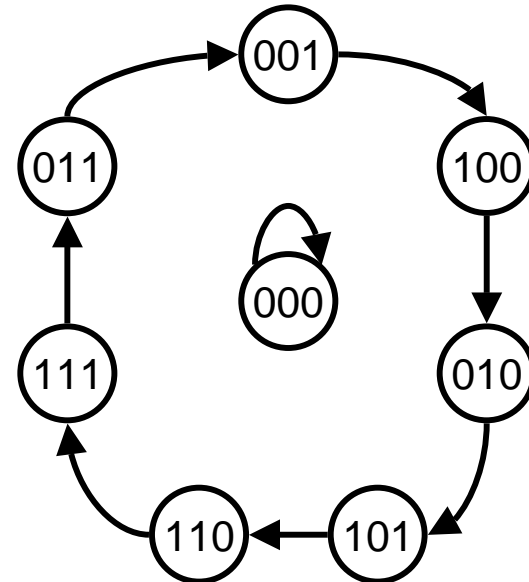
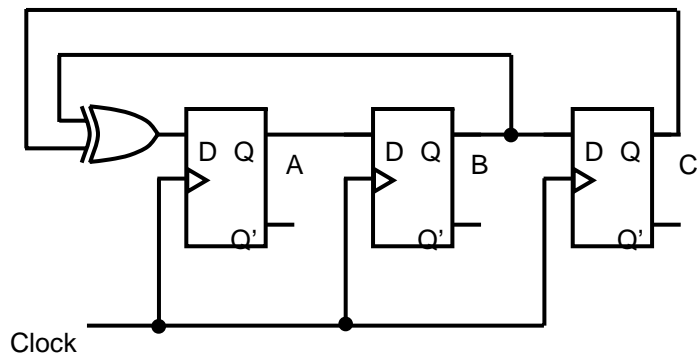
- Description by State Table



Present State			Input	Next State			Output
A	B	C	-	A	B	C	-
0	0	0	-	0	0	0	-
0	0	1	-	1	0	0	-
0	1	0	-	1	0	1	-
0	1	1	-	0	0	1	-
1	0	0	-	0	1	0	-
1	0	1	-	1	1	0	-
1	1	0	-	1	1	1	-
1	1	1	-	0	1	1	-

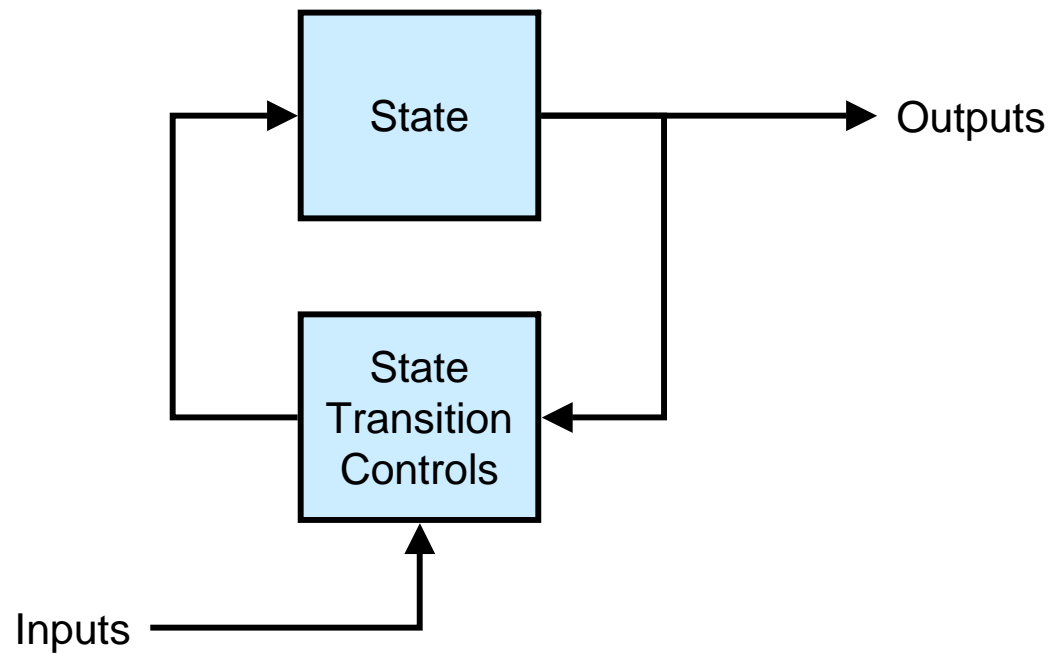
Typical Sequential Circuit With No Inputs

- Description by State Diagram



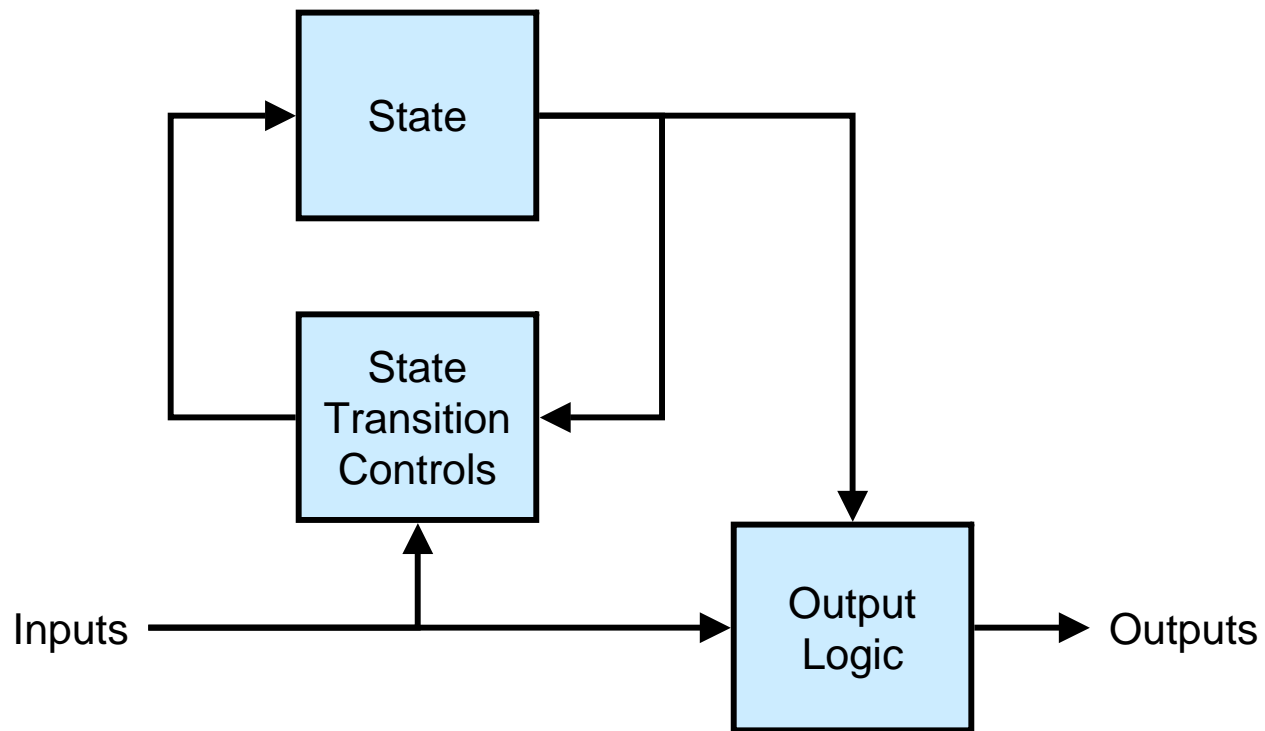
Mealy/Moore Models

- Output is a function of state only = Moore Model



Mealy/Moore Models

- Output is a function of state and inputs = Mealy Model



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Homework 6 – due in Class 8

- As always, show all work
- Problems 5-6, 5-8, 5-9