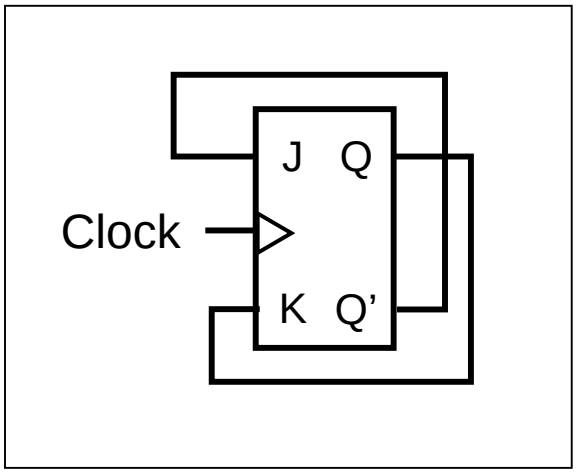
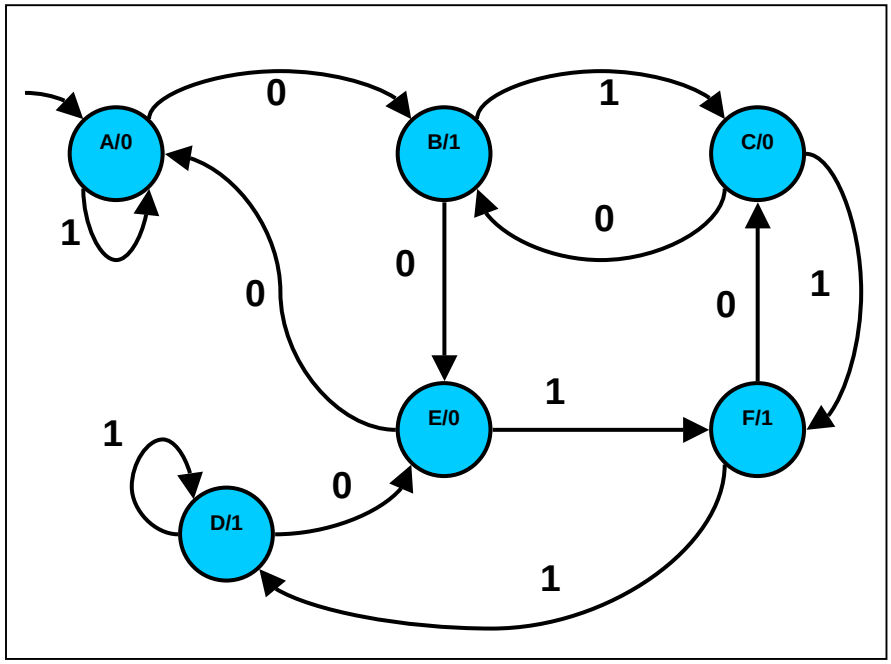
Quiz 2 for CpE358/CS381 – Switching Theory and Logical Design Stevens Institute of Technology Summer 1, 2004 June 9, 2004	Name
Pledge:	
This quiz is open book/open notes. PCs are permitted to lookup information in your notes for the course, but electronic communications with others in the class or outside is prohibited. Total value is 100 points (10% of course grade). All questions are equally weighted ($10.A_{16}$ points each). Do any 6 of the 9 questions. Do more than 6 for extra credit. Some question can be answered in more than one way. Only one answer is required, but extra credit will be given for identifying and explaining alternate answers. Some questions ask for N answers. Extra credit will be given for more than N answers.	

(1) The connections of a J-K flip-flop are shown in the diagram below. If the flip-flop is initially in state 1, what state is the flip-flop in after two clock pulses are received?



State=1 means Q=1, Q'=0, so the JK inputs are 01. This causes the FF to go to the 0 state. State=0 means Q=0, Q'=1, so the JK inputs are 10. This causes the FF to go the 1 state.

(2) The state diagram for a sequential circuit is shown in the figure below. If the system starts in State A, what states does the system go through if the input sequence is 101001010?



A-A-B-C-B-E-F-C-F-C

(3) Write the state table for the state diagram of problem (2)

State	Input	Next state	Output
A	0	B	0
A	1	A	0
B	0	E	1
B	1	C	1
C	0	B	0
C	1	F	0
D	0	D	1
D	1	E	1
E	0	A	0
E	1	F	0
F	0	C	1
F	1	D	1

(4) The sequential circuit shown below has a clock signal as its only input.

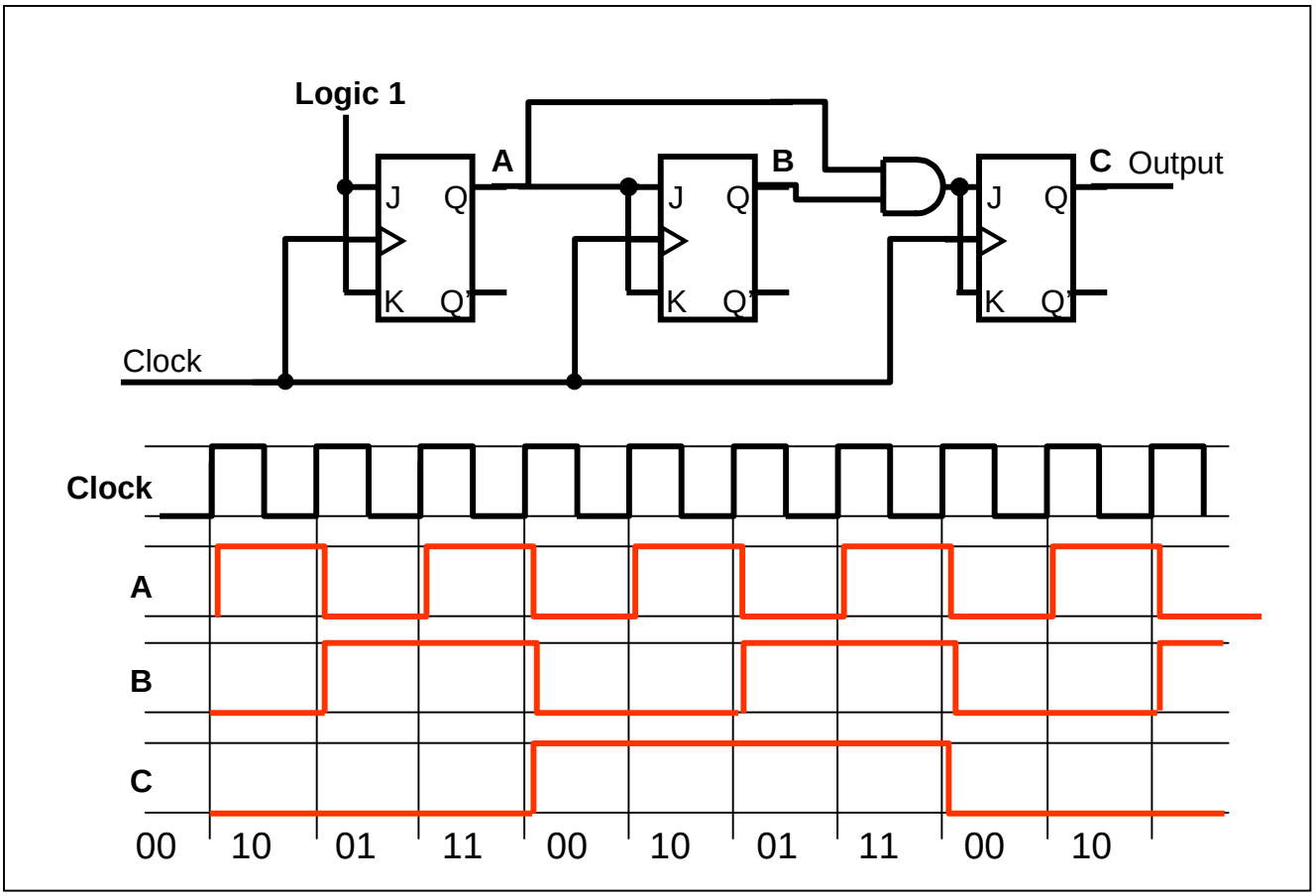
a. If the system starts in the state 000, what are the next 9 states it goes through?

b. If the output is C, what function is this circuit performing?

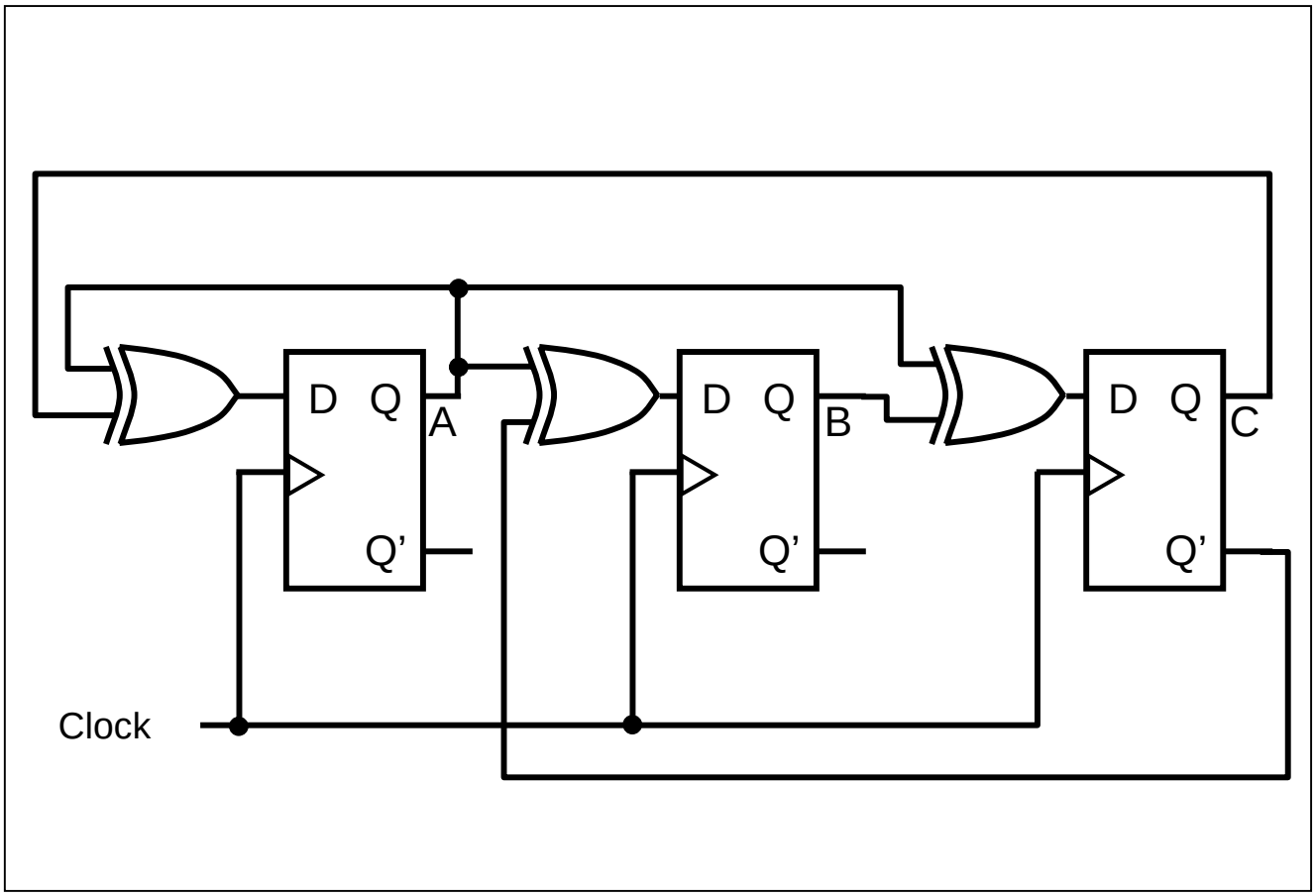
Clock	State	Output
0	000	0
1	100	0
2	010	0
3	110	0
4	001	1
5	101	1
6	011	1
7	111	1
8	000	0
9	100	0

a. 000-100-010-110-001-101-011-111-000-100

b. This circuit is dividing the clock input frequency by 8

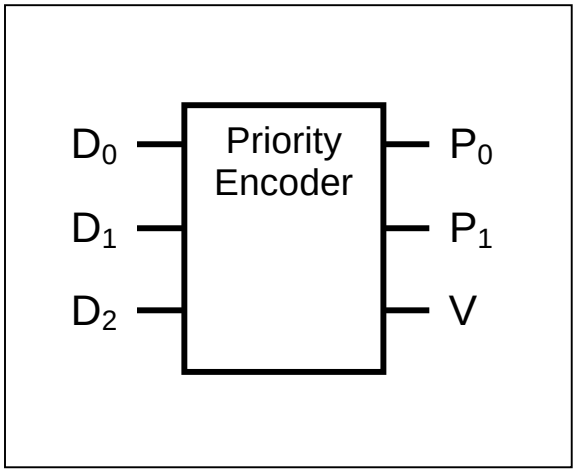


(5) Write the state equations for the following sequential circuit:



$$A(t+1) = A(t) \oplus C(t)$$
$$B(t+1) = A(t) \oplus C'(t)$$
$$C(t+1) = A(t) \oplus B(t)$$

(6) Design a 3-input Priority Encoder: $P_1P_0 = 00$ if D_0 is the first input that is asserted; $P_1P_0 = 01$ if D_1 is the first input that is asserted; $P_1P_0 = 10$ if D_2 is the first input that is asserted. V=0 if no inputs are asserted.



First, write the truth table

D_0	D_1	D_2	P_0	P_1	V
0	0	0	X	X	0
1	X	X	0	0	0
0	1	X	1	0	1
0	0	1	0	1	0

Then draw the three 3-variable Karnaugh Maps:

P_0:

D_1D_2	00	01	11	10
D_0=0	X	0	1	1
D_0=1	0	0	0	0

$P_0=D_0'D_1$

P_1:

D_1D_2	00	01	11	10
D_0=0	X	1	0	0
D_0=1	0	0	0	0

$P_1=D_0'D_1'$

V:

D_1D_2	00	01	11	10
D_0=0	0	1	1	1
D_0=1	1	1	1	1

$V=(D_0D_1D_2)'$

(7) Perform the following conversions:

a. $(A4D7.56)_{16} = (?)_8$
b. $(2570.625)_{10}=(?)_2$
c. $(-192)_{10}= (?)_{16}$ (use 16-complement with 3 hexadecimal digits)

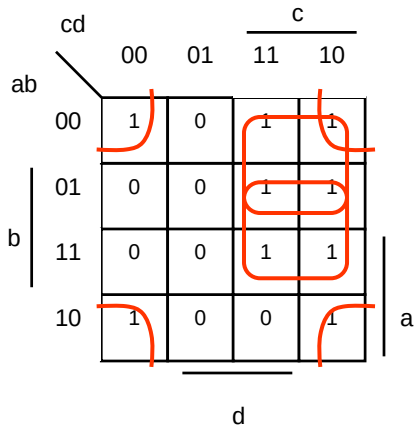
a. $(A4D7.56)_{16} = (?)_8$
   $(A4D7.56)_{16}=(1010\ 0100\ 1101\ 0111.0101\ 0110)_2 =$
   $(1\ 010\ 010\ 011\ 010\ 111.010\ 101\ 10\mathbf{0})_2 =$
   $(1\quad 2\quad 2\quad 3\quad 2\quad 7.\quad 2\quad 5\quad 4)_8$
   $(122327.254)_8$

b. $(2570.625)_{10}=(?)_2$
   $(2570.625)_{10} = (257*10 + .625)_{10} = ((256+1)*10 +.625)_{10}=$
   $(100000001 * 1010)_2 + (.5+.125)_{10}=$
   $(101000001010.101)_2$

c. $(-192)_{10}= (?)_{16}$ (use 16-complement with 3 hexadecimal digits)
   $(192)_{10} = (128+64)_{10} = (0000\ 1100\ 0000)_2 =$
   $(0C0)_{16}$
   so, $(-192)_{10} = (F3F+1)_{16} = (F40)_{16}$

   An alternative way to do this is:
   $(-192)_{10} = (1111\ 0011\ 1111 + 1)_2 = (1111\ 0100\ 0000)_2 =$
   $(F40)_{16}$

(8) Simplify the following Karnaugh map (covering 1's) and define the function it represents in terms of the combinatoric expression:



F(a,b,c,d) = a'c + b'd' + bc

(9) Design a serial adder/subtractor. Assume there are momentary "ADD/SUBTRACT" pulse inputs, followed by a signal that indicates that the data stream has begun that both precede the data streams.