

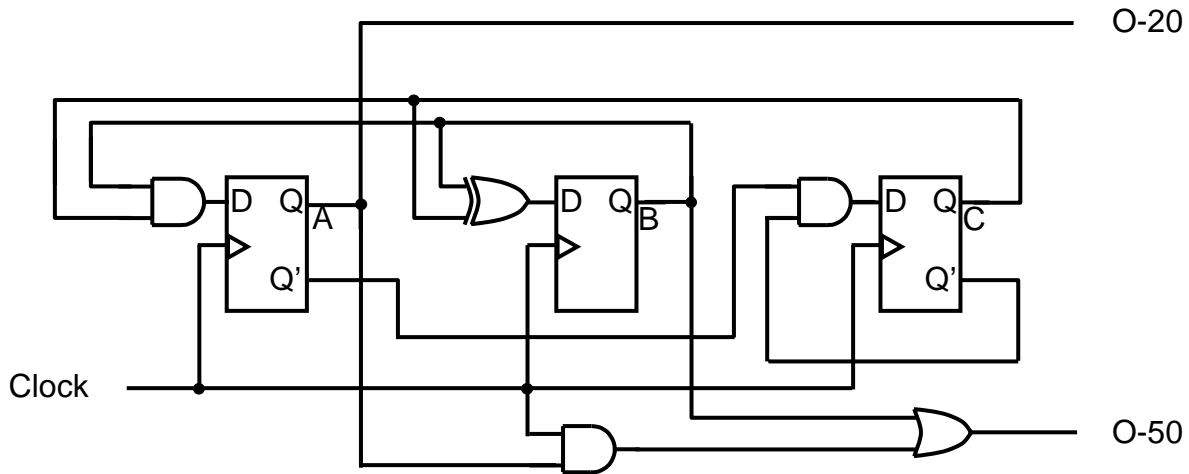
Quiz 4 for CpE358/CS381 – Switching Theory and Logical Design Stevens Institute of Technology Summer 1, 2004 June 23, 2004	Name
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Pledge:

This quiz is open book/open notes. PCs are permitted to lookup information in your notes for the course, but electronic communications with others in the class or outside is prohibited.

Total value is 100 points (10% of course grade). All questions are equally weighted. Do any 5 of the 6 questions. Do more than 5 for extra credit. Some question can be answered in more than one way. Only one answer is required, but extra credit will be given for identifying and explaining alternate answers. Some questions ask for N answers. Extra credit will be given for more than N answers.

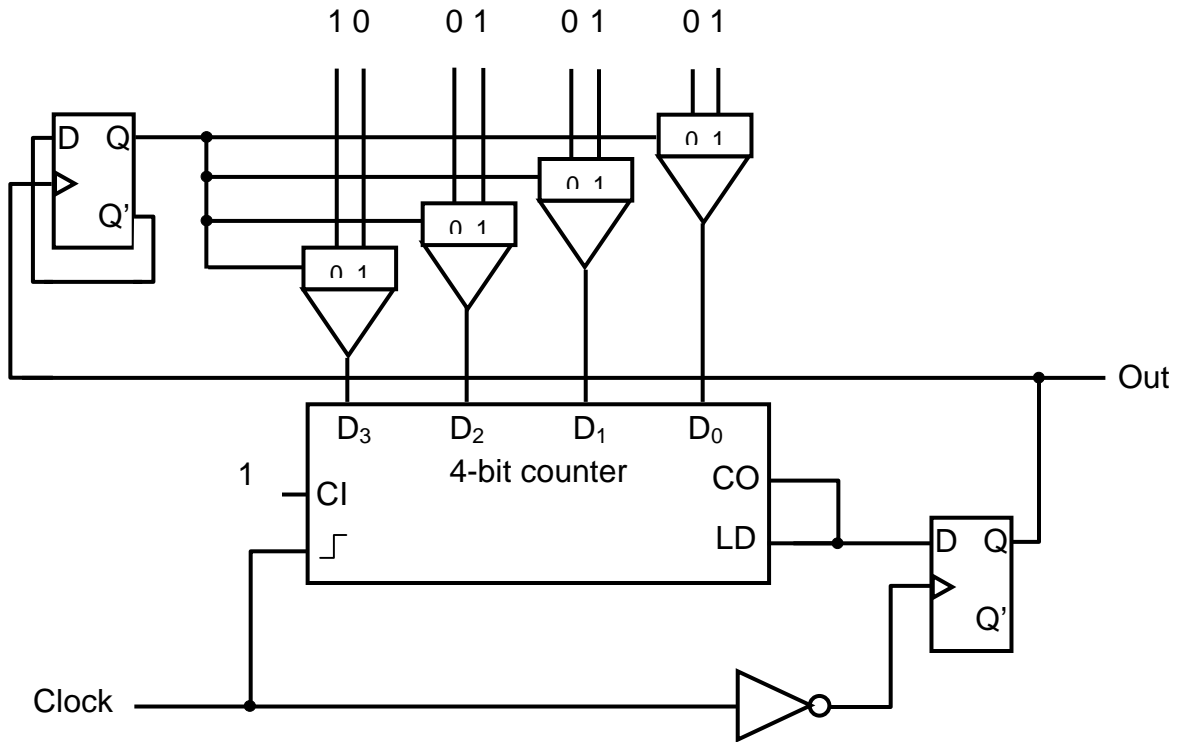
(1) The circuit below is a divide by 5 counter. Output O-20 is a pulse that is asserted  $1/5^{\text{th}}$  of the time, while output O-50 has a 50% duty cycle (it is asserted 50% of the time). Some applications require clocks with 50% duty cycles, so this is a necessary feature of the signal. What issues might exist with outputs O-20 or O-50 and (extra credit) how could they be avoided?



The clock signal ANDed with the A output could occur after the transition in the B output from 1 to 0. If this happens, there will be a short glitch in the O-50 signal.

This could be avoided by generating a copy of B that is delayed slightly. It is important to maintain the leading edge of B, but the trailing edge can occur any time before the falling edge of the clock. In general this is not a desirable way to design synchronous logic, but there is no practical way to generate a 50% duty cycle clock when dividing by an odd number.

(2) An N-bit programmable synchronous counter can generally divide by any number K, where K ranges from 2 to  $2^N$ . This is performed by loading  $2^N - K$  into the data inputs of the counter. Describe the sequence of states of the 4 bit counter shown below. What function is this circuit performing?



This circuit alternately loads 7 or 8, so it is dividing by either 9 or 8. On average, this will appear to be a divide by  $8\frac{1}{2}$ . The D FF on the right clocks the Carry Out on the negative edge, so it is immune from the decoding glitch that might exist at the transition from state 11 to 12. The output signal will be a pulse that occurs every 8 or 9 clock pulses. The D FF at the upper left is acting like a toggle FF, alternating between 0 and 1 for each Carry Out pulse. This causes the two input selectors to alternately load either 7 or 8 after each Carry Out pulse. Since the carry out pulse causes the load on the positive edge, and the D FF changes the load value on the negative clock edge, we are assured that the data will always be stable when it is loaded.

(3) An asynchronous circuit has the excitation functions:

$$Y_1 = x_1x_2 + x_2y_1 + x_2y_2' + x_1'y_1y_2'$$

$$Y_2 = x_1'y_1 + x_2y_1y_2 + x_1'x_2y_2' + x_1'x_2'y_2$$

Find the transition table and indicate the stable states.

Here is the transition table. The stable states are marked in red

		$x_1x_2$			
		00	01	11	10
$y_1y_2$	00	00	11	10	00
	01	01	00	10	00
	11	01	11	11	00
	10	11	11	10	00

- (4) An asynchronous circuit has the transition table shown below. Under what conditions might this circuit have stability issues?

		$X_1X_2$			
		00	01	11	10
$y_1y_2$	00	00	11	10	11
	01	11	00	10	01
	11	10	10	11	00
	10	10	11	10	01

With input 01, there are no stable states (states which have the same  $Y_1Y_2$  value as the  $y_1y_2$  value).  
From state 00, input 10 causes a transition to state 11, which leads back to 00, creating an unstable condition.

- (5) Identify at least one race conditions that exists in the transition table of problem (4). Identify if the race is critical or not. (extra credit for identifying more than 1)

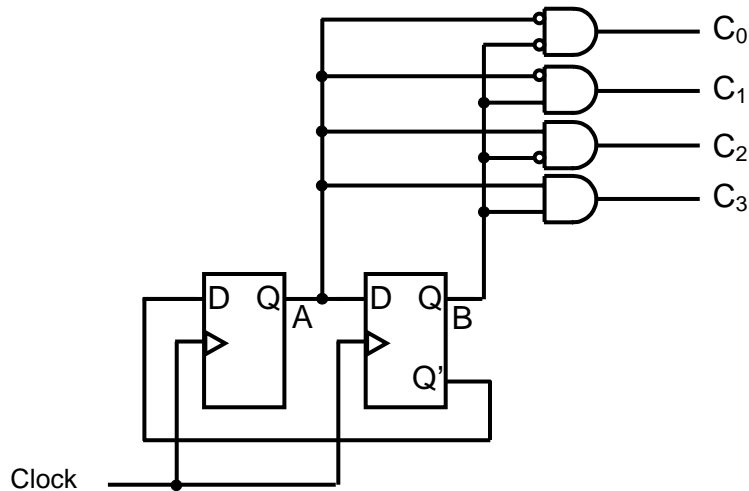
In state 01 with input 10, the system is in a stable state. If the input changes to 11, the next state is 10, requiring change of two state variables. The transitory state might be 00, 10 or 11. If the transitory state is 00, this sends the system to state 10, a stable state. Likewise, if the system goes directly to state 10, this is a stable state. However, if the transitory state is 11, with input 11, this is a stable state, so we have a critical race.

In state 11 with input 11, the system is in a stable state. If the input changes to 10, the next state is 00, requiring change of two state variables. The transitory state might be 01, 10, or 00. If the transitory state is 01, this is a stable state. If the transitory state is 10, with input 10, this causes a transition to state 01. Thus there is a race, but it is not critical. However, if the system goes directly to state 00, the next state is 11, the state we just came from. If the two state variables again change at the same instant, the system will return to state 11, creating an unstable condition. If one of the state variables changes first when going from state 00 to 11, we will again stabilize in state 01, perhaps visiting state 10 briefly.

In state 00 with input 00, the system is in a stable state. If the input changes to 10, the next state is 11, requiring change of two state variables. The transitory state might be 01 or 10. If the transitory state is 01, this is a stable state. If the transitory state is 10, with input 10, this causes a transition to state 01. Thus there is a race, but it is not critical. Like the case above that starts in state 11, there is the potential for instability if the two state variables continue to change at the same time.

In state 10, with input 00 or 11, the system is in a stable state. If the input changes to 10, the next state is 01, requiring change of two state variables. The transitory state might be 00, 01 or 11. If the transitory state is 01, this is a stable state. However, if the transitory state is 00 or 11, this causes a transition to state 11 or 00, respectively. As above, if this simultaneous transition continues, the system will oscillate between state 00 and 11.

- (6) The circuit below is intended to generate sequential, non-overlapping clock pulses. Identify any issues that might exist with this circuit and suggest how it could be improved.



First, the outputs are not numbered in order of the timing of the pulses. If the state of the D FFs is AB, the sequence of states will be 00, 10, 01, 11. The outputs should be labeled (from top to bottom): C<sub>0</sub>, C<sub>2</sub>, C<sub>1</sub>, C<sub>3</sub>. In addition, there is a potential for glitches in the outputs of the AND gates. For instance, as the state changes from 11 to 00, if A changes before B, there will be a glitch in the C<sub>1</sub> output. Likewise, if B changes before A, there will be a glitch in the C<sub>2</sub> output. Generally, there can be glitches expected in all the outputs at one point or another.

This could be addressed in one of four ways.

1. Each output could be retimed on the negative edge of the clock. This would require 4 additional FFs.
2. A ring counter consisting of 4 FFs and no other logic could be used.
3. Additional gates could be added to cover the states at the transitions. Remember, the glitch is caused by a hazard, where the system is transitioning between two states. In this case, we could cover the zeros in the Karnaugh map and ensure that there were no uncovered transitions.
4. Often designers will add inverters to delay some of the signals to prevent glitches. This is usually a solution that is doomed to failure, as the delays may change with temperature or power supply voltage. It is generally not wise to use this method to prevent glitches.